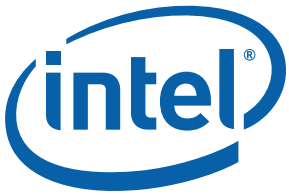

Intel® System Controller Hub (Intel® SCH)

Specification Update

April 2008

Notice: The Intel® SCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Document Number: 319538-001US

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Revision History

Revision Number	Description	Revision Date
-001	Initial release	April 2008

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Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Number
Intel® System Controller Hub (Intel® SCH) Datasheet	319537-001US

Nomenclature

Errata are design defects or errors in engineering samples. These may cause the Intel® SCH behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® SCH. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification change or clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Note: Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Stepping	Status	Description
	D1		
1	X	No Fix	Audio Pops With High LPC Traffic
2	X	No Fix	System Hang With PCIe Upstream Memory Write To FEE00000 With No Data
3	X	No Fix	PCIe PLL May Not Power Down In L1 State
4	X	No Fix	EHCI Controller - Unable To Mask Wake Events Per Port
5	X	No Fix	PCIe Controller Fails To Go Into L1 State In Some Configurations
6	X	No Fix	High Definition Audio Does Not Send Interrupts to the CPU via MSI
7	X	Plan Fix	Incorrect TPM Access
8	X	No Fix	LPC Prefetch Outside of FWH Region
9	X	No Fix	PATA Max Slew Rate Spec Violation
10	X	Plan Fix	USB Client Drops Data Which Causes CRC Errors in Full-Speed Mode
11	X	No Fix	System Hang During PCI Config Space Access

Specification Changes

No.	SPECIFICATION CHANGES
	There are no specification changes in this revision of the specification update.

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications in this revision of the specification update.

Documentation Changes

No.	DOCUMENTATION CHANGES
	There are no documentation changes in this revision of the specification update.

Identification Information

Stepping	S-Spec	MM#	QDF #	Product	Notes
D1	SLB4U	897637	QT52	AF82US15W	Thin Core (2.08 mm Package Height)
D1	SLB4V	897638	QT53	AF82US15L	Thin Core (2.08 mm Package Height)
D1	SLB4W	897636	QT54	AF82UL11L	Thin Core (2.08 mm Package Height)

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Device and Revision Identification

7 Host Bridge (D0:F0)

7.2.2 DID—Identification Register

Device: D0:F0
Offset: 02h–03h
Default Value: 810xh
Attribute: RO
Size: 16 bits

Bit	Default and Access	Description
15:0	8100-8107h RO	**Device ID (DID):** This is a 16-bit value assigned to the controller. The lower 3 bits of this register are determined by fusing. Component: UL11L, DID: 8101 Component: US15L, DID: 8101 Component: US15W, DID: 8100

9 Graphics, Video, and Display (D2:F0)

9.4.2 DID—Device Identification Register

Device: D2:F0
Register Address: 02h
Default Value: 8108h
Attribute: RO
Size: 16 bits

Bit	Default and Access	Description
15:0	8108-810Fh RO	**Device Identification Number (DID):** The lower 3 bits of this register are determined by a fuse. 000b for the UMPC SKU and 001 for MID SKU. Component: UL11L, DID: 8109 Component: US15L, DID: 8109 Component: US15W, DID: 8108

17 LPC Interface (D31:F0)

17.2.5 RID—Revision Identification Register

Device: D31:F0
Offset: 08h Attribute: RO
Default Value: See bit description Size: 8 bits

Bit	Default and Access	Description
7:0	RO	**Revision ID (RID):** Matches the value of the RID register in the LPC bridge. RID: 06 — Qual. Sample: QS — Stepping: D1

Intel® SCH Component High-Level Feature Comparison

Description	US15W	US15L	UL11L
External Graphics (on PCI Express*)	Enabled	Enabled	Disabled
HW Video Decode HD Support	High Definition	High Definition	Standard Definition
SDVO 2nd Display port	Enabled	Enabled	Disabled
Gfx or Display SW capability (LVDS Internal Display Resolution)	0 = All resolutions supported on internal display	0 = All resolutions supported on internal display	1 = Max display resolution on internal display limited to 800x480
DRAM Clock pairs	SM_CK1, SM_CK0	SM_CK1, SM_CK0	SM_CK0
DDR/FSB Frequency	533/400 MHz	533/400 MHz	400 MHz
Memory ranks supported	2	2	1
PCI Express	Port 0,1	Port 0,1	Port 0 only
Graphics Frequency	200 MHz	200 MHz	100 MHz effective
TDP[1]	2.3 W	2.3 W	1.6 W

NOTES:
1. Assumes six USB ports, PCI Express ports support L0s.

Errata

1. Audio Pops With High LPC Traffic

Problem: Audio under-run during high LPC traffic

Implication: Momentary audio streaming interruption

Workaround: None. LPC utilization is fairly low after BIOS has been shadowed and should not affect audio play back.

Status: For the steppings affected, see the Summary Tables of Changes.

2. System Hang With PCIe Upstream Memory Write To FEE00000 With No Data

Problem: When a PCI Express device initiates a FFE00000 write with all byte enable disabled, the SCH turns it into a MSI write, but the SCH continues to wait for the data payload that does not exist.

Implication: System may hang. This is a PCI Express compliance violation.

Workaround: None. A downstream devices should not initiate this type of transactions.

Status: For the steppings affected, see the Summary Tables of Changes.

3. PCIe PLL May Not Power Down In L1 State

Problem: The power management logic in the PCIe unit fails to power down the PLL when one of the PCIe port is in function disable and the other port is in L1 state.

Implication: A potential loss of ~100mW power savings if one of the PCIe port is in function disable.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

4. EHCI Controller - Unable To Mask Wake Events Per Port

Problem: The Controller cannot mask any ports against EHCI wake events.

Implication: Any EHCI port can cause system to wake

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

5. PCIe Controller Fails To Go Into L1 State In Some Configurations

Problem: If PCIe port 1 is populated and PCIe port 0 is not populated, both PCIe ports fail to go into L1 state to reduce power.

Implication: Fails to recognize an estimated power saving of approx. 100mW

Workaround: If only one PCIe port is needed in a design, use Port 0 and function disable Port 1. If 2 PCIe ports exist on the platform, use port 0 first.

Status: For the steppings affected, see the Summary Tables of Changes.

6. High Definition Audio Does Not Send Interrupts to the CPU Via MSI

Problem: The HDA unit cannot send interrupts to the CPU via MSI.

Implication: OS or media applications will revert to the legacy method to send interrupts.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

7. Incorrect TPM Access

Problem: A host byte read access to the TPM module via the LPC bus causes four single byte reads on LPC instead of a single byte read.

Implication: The TPM module uses a FIFO which after the first host byte 0 read, will be incremented to provide byte 4 upon the next host byte read due the behavior of the SCH. Software is actually expecting the TPM byte 1 to be read upon the second transaction. Third party software stacks will not properly function due to this erratum.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

8. LPC Prefetch Outside of FWH Region

Problem: The SCH has a feature called FWH prefetching and this allows for a 64-byte fetch of the FWH device sitting on the LPC bus. This prefetch option is supposed to be confined to only the address range of the FWH. However, unintentional prefetching may also extend to other addresses.

Implication: Some devices such as TPM modules will return incorrect data because these devices do not allow prefetching.

Workaround: Disable BIOS prefetching by setting D31:F0, offset DBh, bit 8 = 0. Overall boot time may increase. This workaround is only required when using devices that do not allow prefetching such as TPM modules.

Status: For the steppings affected, see the Summary Tables of Changes.

9. PATA Max Slew Rate Specification Violation

Problem: The Intel SCH PATA output buffers may violate the ATA max slew rate spec of 1.0V/ns under fast corner conditions. No violations of Voh/Vol, overshoot or undershoot have been observed.

Implication: This is a specification violation via synthetic load testing only. No functional failures have been observed.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

10. USB Client Drops Data Which Causes CRC Errors in Full-Speed Mode

Problem: CRC errors in customer systems may lower USB performance or cause the connected USB 1.1 host system to disable a USB-client and signal error to end-user. The last byte of a USB packet may be lost and this causes the USB client to detect a CRC error.

Implication: Impact is part dependent and limited to when the client is connected with USB 1.1 hosts only. Some affected parts may have no noticeable impact. CRC errors may cause a port to be reset and retried, but if errors continue and the port is reset three times, the host operating system will disable the client device and flag an error message.

Workaround: Use USB 2.0 host only with the current USB Client driver to continue USB Client application development and validation. The PV USB Client driver will have an infrastructure that the OEM user-mode application can use to take the appropriate action if the client is connected to a full-speed host.

Status: For the steppings affected, see the Summary Tables of Changes.

11. System Hang During PCI Config Space Access

Problem: When the HD audio controllers memory space enable (MSE) register is enabled and a PCI config space cycle which is targeted to some other PCI device occurs that also matches the HD audio controllers memory base address register, the HD audio controller will claim this cycle. There are other conditions required to encounter this erratum: a. HD audio memory BAR (base address register) [31:24] must match the config cycle number and b. HD audio memory BAR [23:19] must match config cycle device number and c. HD audio memory BAR [18:16] must match config cycle function number.

Implication: A system hang may occur as a result of the HD audio controller incorrect claim of the PCI config cycle. This issue was found using a specific PCI bus test compliance software. Typical systems do not have enough PCI busses (greater than 127) to encounter this issue.

Workaround: None

Status: For the steppings affected, see the Summary Tables of Changes.

Specification Changes

There are no specification changes in this revision of the specification update.

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Specification Clarification

There are no specification clarifications in this revision of the specification update.

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Documentation Changes

There are no documentation changes in this revision of the specification update.

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